IN THE FIGURES

Figure 3 is added to the application and is attached to this Preliminary Amendment.

IN THE SPECIFICATION

On page 2, line 39, change "invention." to "invention; and".

On page 2, after line 39, insert text as follows:

--FIG. 3 illustrates an alternate embodiment of a processing circuit for pixel signals in accordance with the present invention.--

On page 6, lines 183-184, change "selected a" to "a selected".

Insert the following text after page 8, line 236, after "as it is received."

--FIG. 3 illustrates a schematic diagram of imaging integrated circuit 26 in an alternate embodiment, including optical sensor 32 and signal processing circuit 34.

Optical sensor 32 includes 2,752 photodetectors coupled to a CDS circuit 168 having 2,752X2=5,504 sample and hold (S/H) amplifiers. In other words, each photodetector is coupled to two S/H amplifiers, a first S/H amplifier sampling the dark level on one transition of SYSCLK and holding the dark level while a second S/H amplifier samples the light level. The dark levels generated by the photodetectors are

concurrently sampled on one SYSCLK transition, and the light levels are sampled on another SYSCLK transition. Hence, the S/H amplifiers perform a correlated double sampling function for the photodetectors.

The dark and light signal levels are provided on separate conductors of bus 38. Hence, bus 38 includes 5,504 conductors to conduct the reference and signal levels for 2,752 photodetectors. By performing the correlated double sampling function in parallel on all of the photodetectors, pixel signals can be processed at a higher rate or, as an alternative, the frequency of SYSCLK can be reduced to reduce switching and other system noise while maintaining the processing rate of pixel signals.

A multiplexer 162 receives pixel addresses on bus 36 to select one of the forty-three regions 52 of sensor 32 in a fashion similar to multiplexer 62 shown in FIG. 2. Hence, the dark and light signal levels on bus 38 are provided at 5,504 inputs of a multiplexer 162. These dark and light signal levels are routed through separate decoding matrices within multiplexer 162 and provided on separate conductors of a bus 171. Hence, multiplexer 162 provides sixty-four dark levels and sixty-four light levels generated within a selected region on to one hundred twenty-eight outputs coupled to a one hundred twenty-eight conductor bus 171.

A one of sixty-four analog multiplexer 163 receives a pixel address on bus 35 and selects from among the dark and light levels of pixel signals within a region 52 selected by multiplexer 162. Multiplexer 163 has 64X2=128 inputs coupled to bus 171 for routing the dark and light levels of selected pixel signals to nodes 161 and 165, respectively.